

CMP-MSI: 2nd Workshop on Chip Multiprocessor Memory Systems and Interconnects

In conjunction with the

[35th International Symposium on Computer Architecture \(ISCA-35\)](#)

Sunday, June 22nd, 2008
Beijing, China

List of Accepted Papers

Full papers

- *Dynamic Parameter Tuning for Hardware Prefetching Using Shadow Tagging* , Marius Grannaes and Lasse Natvig, Norwegian University of Science and Technology.
- *Dynamic Classification of Program Memory Behaviors in CMPs* , Yuejian Xie, Gabriel H. Loh, Georgia Institute of Technology.
- *Double-DIP: Augmenting DIP with Adaptive Promotion Policies to Manage Shared L2 Caches* , Jonathan D. Kron, Brooks Prumo, Gabriel H. Loh, Georgia Institute of Technology.
- *Alternative Home: Balancing Distributed CMP Coherence Directory* , Zhuo Huang (University of Florida), Xudong Shi (Google Inc.), Ye Xia (University of Florida), Jih-Kwon Peir (University of Florida).
- *Extending the Scalability of Single Chip Stream Processors with On-chip Caches* , Ali Bakhoda and Tor M. Aamodt, University of British Columbia.
- *Scalable On-Chip Interconnect Topologies* , Boris Grot and Stephen W. Keckler, The University of Texas at Austin.
- *Perceptron-based Coherence Predictors* , Devyani Ghosh, John B. Carter, Hal Daume III, University of Utah.

Position papers

- *Ultrapformance Wireless Interconnect Nanonetworks for Heterogeneous Gigascale Multi-Processor SoCs* , Danella Zhao, University of Louisiana.
 - *Architecture Supported Synchronization-Based Cache Coherence Protocol For Many-Core Processors* , He Huang, Nan Yuan, Wei Lin, Guoping Long, Fenglong Song, Lei Yu, Yuping Liu, Lei Liu, Yongbin Zhou, Xiaochun Ye, Junchao Zhang, Dongrui Fan, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China.
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